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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/650,719	05/20/1996	JEFFREY S. MAILLOUX	95-0653	2941

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	PAPER NUMBER
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	08/650,719	MAILLOUX ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,33-35,46,48-50,59-61,63 and 64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 33-35, 46, 48-50, 59-61, and 63-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/20/96* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/22/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are presented for examination. This office action is in response to the Appeal Brief filed on 12/22/06.

2. The information disclosure statement (IDS) submitted on 12/22/06 is being considered by the examiner.

3. It is noted that this application appears to claim subject matter disclosed in the co-pending section or related section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending or related applications to avoid possible double patenting (i.e. U.S Pat. No 5966724).

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a timing diagram or s logic diagram of "providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation", "switching mode to a burst mode of operation", "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation", and "providing a new external addresses for every access associated with accessing the

asynchronously-accessible memory device while in the burst mode of operation" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

DOUBLE-PATENTING

The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 59-60 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 36 of copending Application No. 08/984,563. Although the conflicting claims are not identical, they are not patentably distinct from each other because both sets of claims are related to a method of accessing a storage device, comprising: a first address, burst and pipelined mode, selecting inputting and outputting information, selecting a burst mode and a pipelined mode, utilizing a second address to access data in a memory. Both sets of claims recited similar inventive concept of accessing a memory in burst and pipelined mode except: Claims 59-60 of the present invention comprises less specific steps than as claimed in the Application No. 08/984,563. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize teaching of 08/984,563 and modify an external row address to a first address and a first external column address to a second address of the copending application to arrive invention of the present application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 61 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Because although the specification (pg.27, 1-11; pg.38, line 11-15; and pg. 39, lines 9-16) describes burst and pipeline operations as pointed out by the applicants in the brief, the specification does not specifically describe claimed limitation of "providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation", "switching mode to a burst mode of operation", "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation", and "providing a new external addresses for every access associated with accessing the asynchronously-accessible memory device while in the burst mode of operation". This instant application describes "switching between burst EDO and pipelined EDO modes is accomplished on successive /CAS cycles" (Pg 38 lines 11-15

and See Fig. 17 Refs 114 and 115, each /CAS cycle represents a new column address in pipeline mode). In other words, a new external address (Fig. 17 3rd addr) is needed after the initial external address (Fig. 17 2nd addr) to switch modes (also refer to claim 46 of the present application), however, applicant claimed generating at least one subsequent internal address patterned without a new external address. Therefore, "providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation", "switching mode to a burst mode of operation", "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation", and "providing a new external addresses for every access associated with accessing the asynchronously-accessible memory device while in the burst mode of operation" were not described in the specification. Again pg. 33, lines 13-21, pg 38, lines 11-15, and pg. 27, lines 5-11 of this instant application do not specifically disclose "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation".

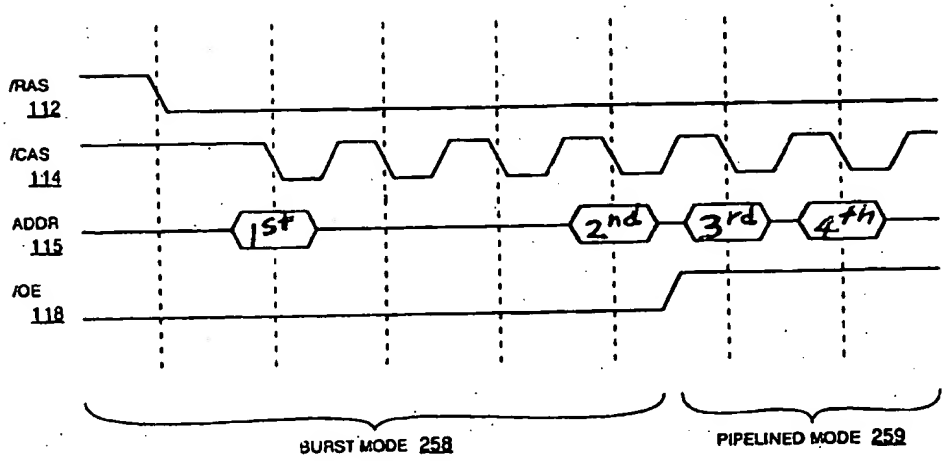
/RAS
112
/CAS
114
ADDR
115
/OE
118
1st
2nd
3rd
4th
BURST MODE 258
PIPELINED MODE 259

FIG. 17

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-9, 33-35, 46, 48-50, 59-60, and 63-64 are rejected under 35 U.S.C. 103(a) as obvious over by *Manning*, U.S. Patent 5,610,864 in view of Roy U.S. Patent No. 6,065,092 or *Ogawa* U.S. Patent 5,293,347.

As to claim 50, *Manning* discloses the invention as claimed. *Manning* discloses a system comprising: a microprocessor (Fig. 11 Ref. 112); a memory (Fig. 11 Ref. 124) coupled to the microprocessor, the memory selectively operable either in a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) or a EDO page mode of operation (col. 6 lines 14-21 and col. 7 lines 40-55), wherein the memory is an asynchronous dynamic random access memory (Fig. 1 and EDO constitutes asynchronous memory, col. col. 6 lines 14-16, since the EDO does not require a system clock to operate); and a system clock (col. 8 line 46) coupled to the microprocessor.

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel

architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 63, *Manning* discloses a storage device, comprising; an array of memory cells (col. 4 lines 13-15); mode circuitry for receiving a burst/page signal (col. 6 lines 14-26 and col. 7 lines 40-55); and operation circuitry operable in a burst or a EDO page mode of operation depending upon the burst/page signal, the operation circuitry

switchable between burst and page modes of operation (col. 5 lines 41-50, col. 6 lines 14-34, and col. 7 lines 40-55).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline signal/mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline signal/mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe.

Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline signal/mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline signal/mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page signal/mode of Manning to a pipeline signal/mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline signal/mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline signal/mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page signal/mode of Manning to a pipeline signal/mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 1, *Manning* discloses the invention as claimed. *Manning* discloses an asynchronously accessible storage device (Fig. 1 and EDO constitutes asynchronous memory, col. col. 6 lines 14-16, since the EDO does not require a system clock to operate) comprising mode circuitry to select between a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) and a EDO page mode (col. 6 lines 14-21 and col. 7 lines 40-55); and circuitry operable in either the burst mode or the page mode coupled to the mode selection circuitry and configure to select between two modes.(Fig. 1 Ref. 40 and col. 6 lines 14-21, col. 5 lines 41-50, and col. 7 lines 40-55).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write,

memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable

feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 2, Manning further discloses the burst mode and the pipelined mode are EDO modes of operation (col. 5 lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54)

As to claim 3, Manning further discloses the pipelined mode is an EDO mode (col. 5 lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54).

As to claim 4, Manning further discloses the burst mode is and EDO mode (col. 6 line 15).

As to claim 5, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 6, Manning further discloses the mode circuitry includes at least one counter for incrementing the address (Fig. 1 Ref. 26 and col.5 lines 51-62).

As to claim 7, Manning further discloses the mode circuitry includes receiving an external address (Fig. 1 Ref. 16 and col. 4 lines 16-28).

As to claim 8, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 9, Manning further discloses the mode circuitry includes multiplexed device for providing an internally generated address to the storage device (Fig. 1 Refs. 26 and 30 and col. 5 lines 51-62 & col. 3 lines 20-23, selection of external or internal address reads on this limitation).

As to claims 33, 59, and 60, *Manning* discloses a method for accessing a storage device (Fig. 1), comprising: receiving a first address to the storage device (Fig. 2 ROW); selecting between an asynchronously accessible (Fig. 1 and EDO constitutes asynchronous operation, col. col. 6 lines 14-16) burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a EDO page mode (col. 6 lines 14-21 and col. 7 lines 40-55); selecting between outputting information from the storage device and inputting to the storage device (Fig. 2 /WE, read and write operations read on this limitation); obtaining a second address to the storage device (Fig. 2 /COL), and asynchronously accessing a storage element of the storage device in the selected mode of operation using the first

address and the second addresses (Fig. 2, DQ and col. 5 lines 41-50, col. 6 lines 14-26 & col. 7 lines 43-54).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe.

Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 34, Manning further discloses a step of switching between the pipelined mode and burst mode (col. 5 lines 41-50, col. 6 lines 14-16 and col. 5 lines 42-50).

Roy also further discloses a step of switching between the pipelined mode and burst mode (col. 27 lines 35 thru col. 28 lines 48 and col. 21 lines 61-62 specifically col. 27 lines 54-58)

As to claim 35, Manning further discloses the second address is an external address (Fig. 1 Refs 16 and 30 and col. 4 lines 16-28 & col. 5 lines 42-55). Roy also further discloses the second address is an external address (col. 28 lines 16-25).

As to claim 46, *Manning* discloses a method for accessing several different locations in an asynchronously a storage device (Fig. 1 and EDO constitutes asynchronous operation, col. col. 6 lines 14-16), comprising: selecting a EDO page mode (col. 6 lines 14-21 and col. 7 lines 40-55); providing a new external address with asynchronously-accessible memory device in the page mode of operation (col. 6 lines 14-21 and col. 7 lines 40-55); switching modes to a burst mode of operation (col. 6 lines 14-21 and col. 7 lines 40-55); providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67); and generating at least one

subsequent internal address patterned after the initial external address while in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe.

Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode and providing a new external address for every access associated with asynchronously-accessible memory device in the pipeline mode of operation (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one

of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode and providing a new external address for every access associated with asynchronously-accessible memory device in the pipeline mode of operation of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode and providing a new external address for every access associated with asynchronously-accessible memory device in the pipeline mode of operation (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode and providing a new external address for every access associated with asynchronously-accessible memory device in the pipeline mode of operation of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claims 48 and 49, Roy further discloses column, row, application; fixed access based switching (col. 27 lines 54-58) for the burst mode and the pipelined mode.

As to claim 64, *Manning* discloses a memory circuit, comprising; an array of memory cells (col. 4 lines 13-15); burst/page selection circuitry for determining a burst or a page mode of operation of the memory circuit (col. 5 lines 41-50, col. 6 lines 14-34 & col. 7 lines 40-55); and mode circuitry capable of operation in either a burst mode or a EDO page mode of operation, and switchable between burst and page modes of operation (col. 5 lines 41-50, col. 6 lines 14-34 & col. 7 lines 40-55).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the

pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Allowable Subject Matter

8. Claim 61 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, set forth in this Office action.

Response to Amendment

Applicant's arguments filed on 12/22/06 have been fully considered but they are not persuasive.

A. In response to applicant's argument on pages 9-10 and 14 in the amendment that claim 61 is described in the Application as filed at the time the application was filed has been fully considered but it is not persuasive.

Again pg. 33, lines 13-21, pg 38, lines 11-15, and pg. 27, lines 5-11 of this instant application do not specifically disclose "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation". It appear that pages 27, 36, and 38 only describes individual burst mode operation and pipelined operation. This instant application describes "switching between burst EDO and pipelined EDO modes is accomplished on successive /CAS cycles" (Pg 38 lines 11-15 and See Fig. 17 Refs 114 and 115, each /CAS cycle represents a new column address in pipeline mode). Again applicants are requested to point out this limitation of "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation" **in the drawing and in the specification**.

B. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, *Roy* discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32). *Alternatively, Ogawa* discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

C. In response to applicant's argument on page 12 in the amendment that the cited reference does not disclose switching between a burst mode and a pipelined mode of operation has been fully considered but it is not persuasive.

Manning (864) discloses the limitation of switching between a burst mode and a EDO page mode of operation.

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel

architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline

mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Therefore, prior arts disclose the limitation of switching between a burst mode and a pipelined mode of operation.

C. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., " on the fly", page 13, 3rd paragraph) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

2. This action is a **final rejection** and is intended to close the prosecution of this application. Applicant's reply under 37 CFR 1.113 to this action is limited either to an appeal to the Board of Patent Appeals and Interferences or to an amendment complying with the requirements set forth below.

If applicant should desire to appeal any rejection made by the examiner, a Notice of Appeal must be filed within the period for reply identifying the rejected claim or claims appealed. The Notice of Appeal must be accompanied by the required appeal fee of $500.

If applicant should desire to file an amendment, entry of a proposed amendment after final rejection cannot be made as a matter of right unless it merely cancels claims

or complies with a formal requirement made earlier. Amendments touching the merits of the application which otherwise might not be proper may be admitted upon a showing a good and sufficient reasons why they are necessary and why they were not presented earlier.

A reply under 37 CFR 1.113 to a final rejection must include the appeal from, or cancellation of, each rejected claim. The filing of an amendment after final rejection, whether or not it is entered, does not stop the running of the statutory period for reply to the final rejection unless the examiner holds the claims to be in condition for allowance. Accordingly, if a Notice of Appeal has not been filed properly within the period for reply, or any extension of this period obtained under either 37 CFR 1.136(a) or (b), the application will become abandoned.

3. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

4. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

5. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(571)-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
February 8, 2007